I2C	Sub SYS	Function	Part Number	I2C Spec.	Budget Timing	i2C Slave Address / Write / Read (7-bit mode)	
I2C-0	AP	Cap Touch controller	GT1151	400 Kbps	Yes.	0x5D	Write:0xBA / Read:0xBB
		LCM Gate Drive	RT4801HWSC	400 Kbps	Yes.		
I2C-1 (BC)	AP Sensor Hub	Magnetic Sensor	AK09918C	400 Kbps	Yes.	0x0C	Write:0x18 / Read:0x19
		Ambient Light Sensor Proximity Sensor	CM36558	400 Kbps	Yes.	0x51	Write:0xA2 / Read:0xA3
		Pressure Sensor	BMP280	400 Kbps	Yes.	0x77	Write:0xEE / Read:0xEF
I2C-2 (BC)	AP	Rear Camera	IMX519	400 Kbps		0x1A	Write:0x34 / Read:0x35
			EEPROM	400 Kbps		0x50	Write:0xA0 / Read:0xA1
			AF driver	400 Kbps		0x0C	Write:0x18 / Read:0x19
		Dual cam (B+b) - Main1	S5K2P7	400 Kbps		0x2D	Write:0x5A / Read:0x5B
			EEPROM	400 Kbps		0x50	Write:0xA0 / Read:0xA1
			AF driver	400 Kbps		0x0C	Write:0x18 / Read:0x19
I2C-3	AP	NFC	ST21NFCD	400 Kbps	Yes.	0x08	Write:0x10 / Read:0x11
		Dual cam (B+b) - Main2	OV8856	400 Kbps		0x10	Write:0x20 / Read:0x21
			EEPROM=NA				
			AF driver=NA				
I2C-4 (BC)	AP	Front Camera	S5K2T7	400 Kbps		0x2D	Write:0x5A / Read:0x5B
			EEPROM	400 Kbps		0x52	Write:0xA4 / Read:0xA5
			AF driver=NA				
I2C-5	AP	Reserved					
I2C-6	AP SSPM	Reserved					
I2C-7	AP	Audio Smart PA	MT6660	400 Kbps	Yes.	0x34	Write:0x68 / Read:0x69
		SW Charger	SW Charger	400 Kbps	Yes.		
		CC Detect	RT1715WSC	400 Kbps	Yes.		
		Flash LED 5V Boost	RT4505	400 Kbps	Yes.		

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

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Date	Category	Item
2018.12.14 (V0.1)	Page 04	V0.1 Release
2019.01.11 (V0.2)	Page 12	Add CAM_PDN3(GPIO110) HW pin for Note 12-4: HW pin for DDR type feature in bootstrap
		Delete R1007 and R1012 ext. pull for LP4X eMCP
	Page 13	Add CAM_PDN3(GPIO110)'s Note : No ext. pull for DDR type feature in bootstrap
	Page 69	Add CAM_PDN3(GPIO110)'s Note : No ext. pull for DDR type feature in bootstrap
	Page 21	Add C2106 for VBIF28 cap
	Page 22	Delete R2202

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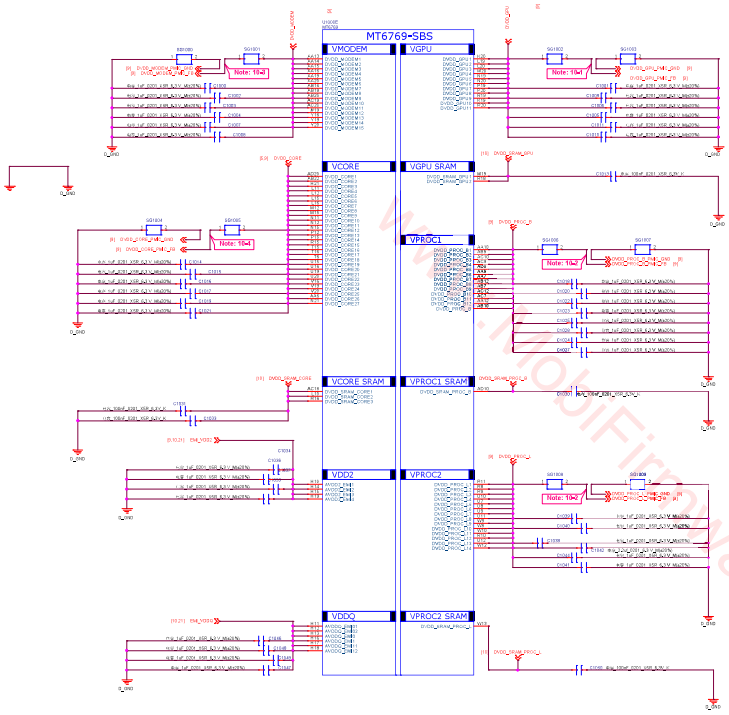

Schematic design notice of "10_BB_ POWER_PDN" page:

Note 10-1:	Differential pair of DVDD_GPU remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-2:	Differential pair of DVDD_PROC remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-3:	Differential pair of DVDD_MODEM remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)
Note 10-4:	Differential pair of DVDD_CORE remote sense must be close to BB's ball. Remote sense trace with GND shielding to PMIC (Differential)

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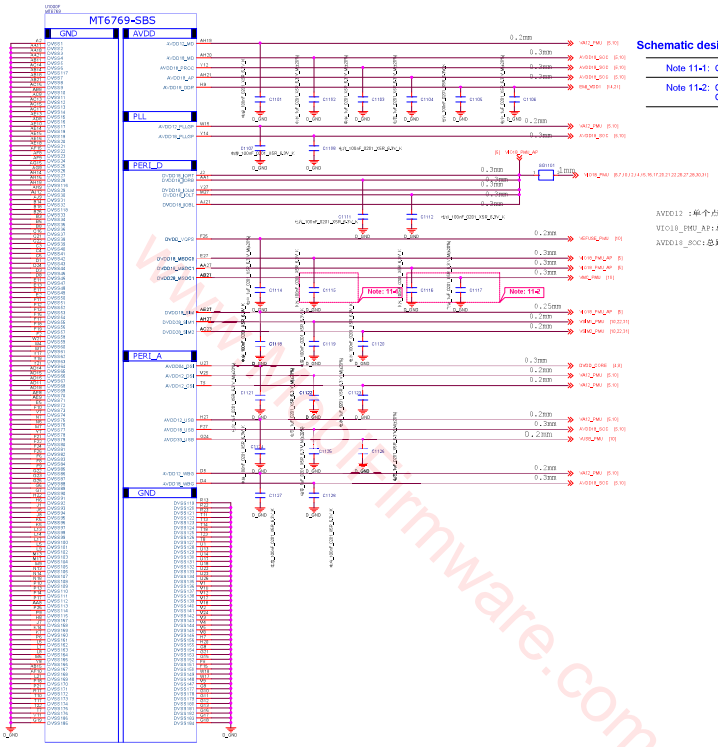

Schematic design notice of "11_BB_POWER_IO" page:

Note 11-1: C1115 closed DVDD18_MSDC0 150mil

Note 11-2: C1116 closed DVDD18_MSDC1 150mil
C1117 closed DVDD28_MSDC1 150mil

AVDD12 :单个点走3mil,两路分支各16mil,总路长20mil
VIO18_PMU_AP:总路长240mil
AVDD18_SOC:总路长20mil

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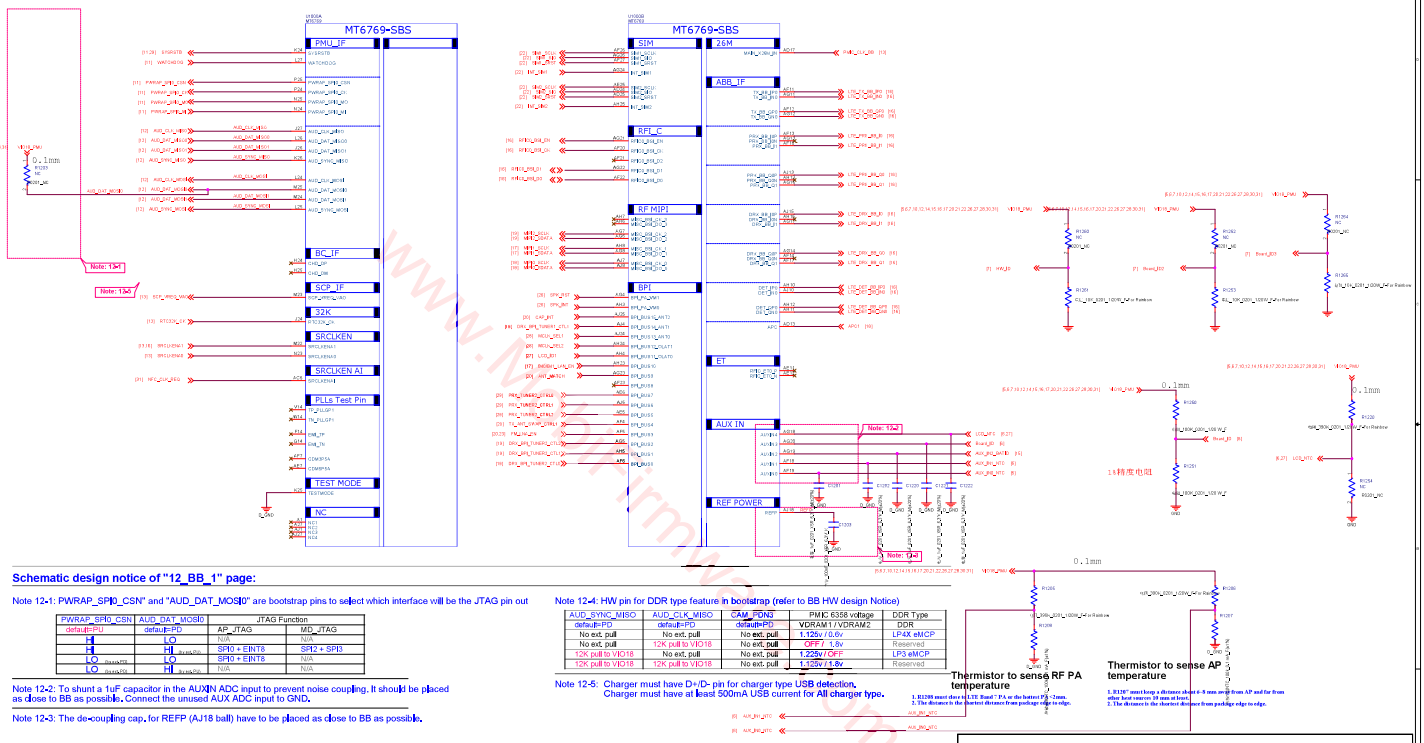

Schematic design notice of "12_BB_1" page:

Note 12-1: PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	JTAG Function	
default=PU	default=PD	AP_JTAG	MD_JTAG
HI	LO	N/A	N/A
HI	HI (default)	SPI0 + EINT8	SPI2 + SPI3
LO	LO	SPI0 + EINT8	N/A
LO (default)	HI (default)	N/A	N/A

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-3: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

Note 12-4: HW pin for DDR type feature in bootstrap (refer to BB HW design Notice)

AUD_SYNC_MISO	AUD_CLK_MISO	CAM_PDN0	PMIC 6358 voltage	DDR Type
default=PD	default=PD	default=PD	VDRAM1/VDRAM2	DDR
No ext. pull	No ext. pull	No ext. pull	1.125v / 0.6v	LP4X eMCP
No ext. pull	12K pull to VIO18	No ext. pull	OFF / 1.8v	Reserved
12K pull to VIO18	No ext. pull	No ext. pull	1.225v / OFF	LP3 eMCP
12K pull to VIO18	12K pull to VIO18	No ext. pull	1.125v / 1.8v	Reserved

Note 12-5: Charger must have D+/D- pin for charger type USB detection.
Charger must have at least 500mA USB current for All charger type.

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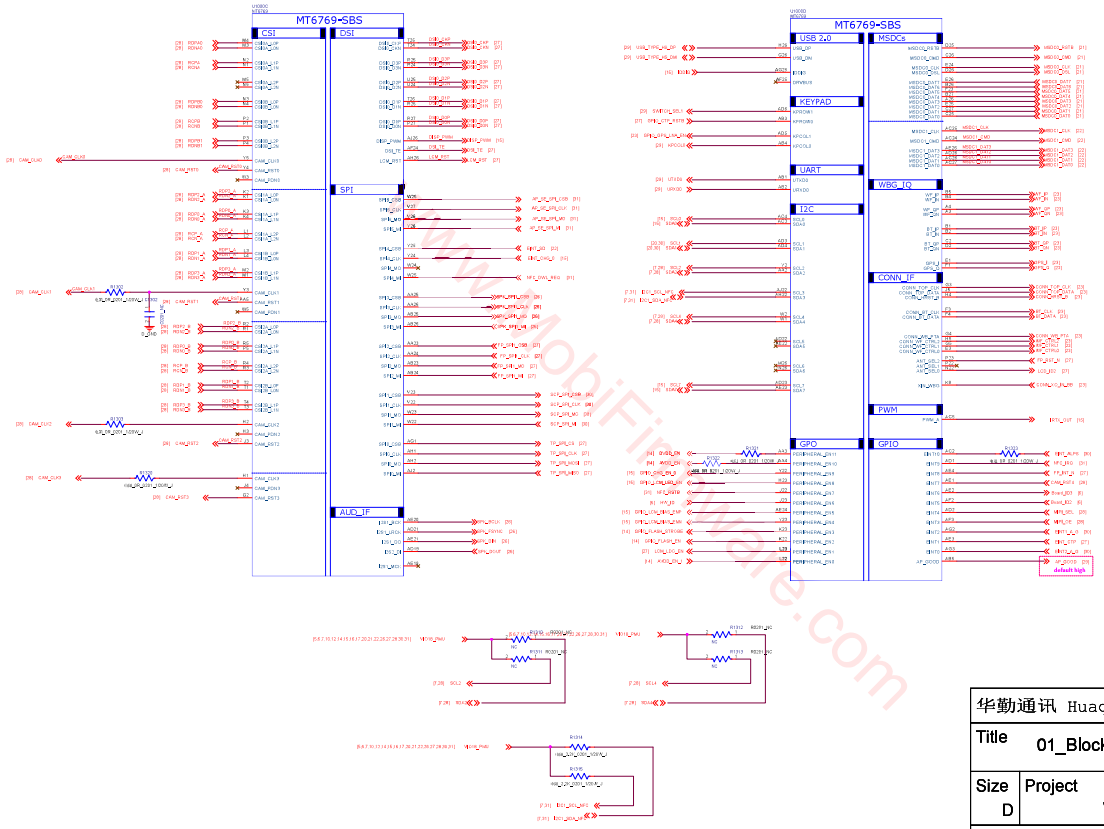

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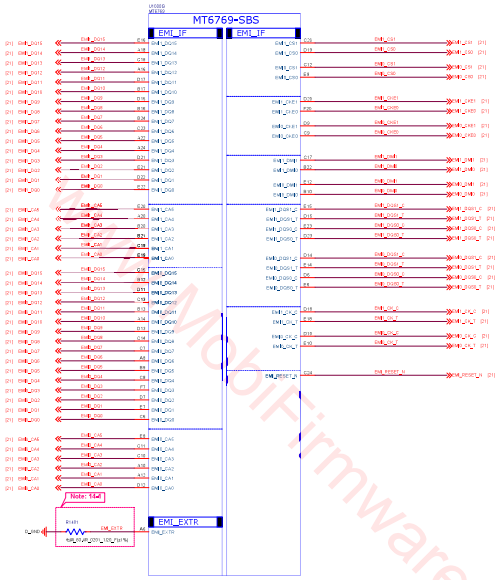

Schematic design notice of "14_BB_3" page.

Note 14-1: R1401 please select 60.4 ohm (1%) resistor

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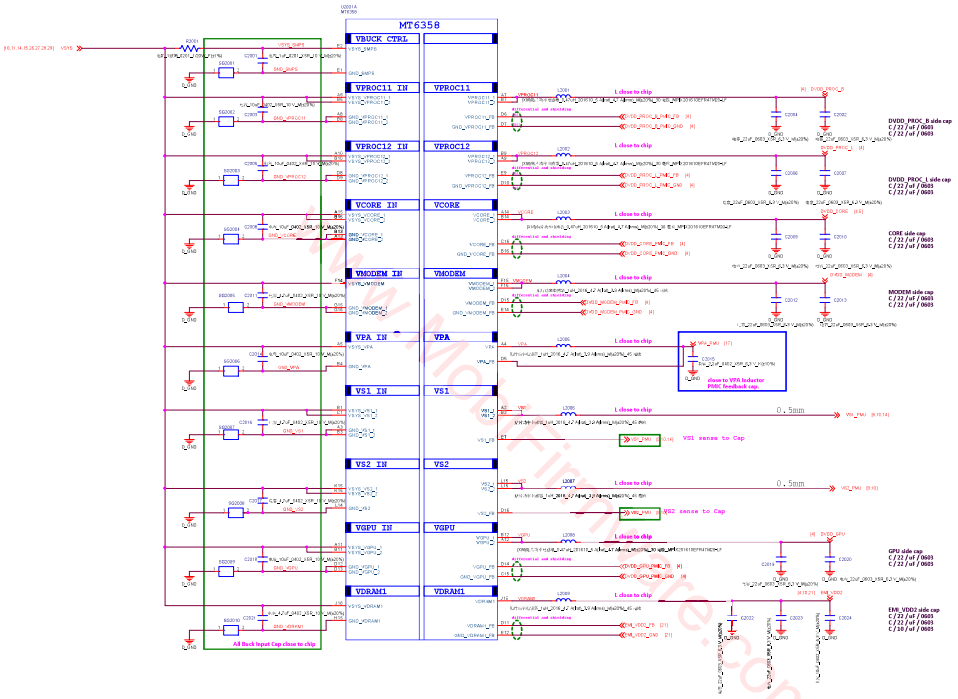

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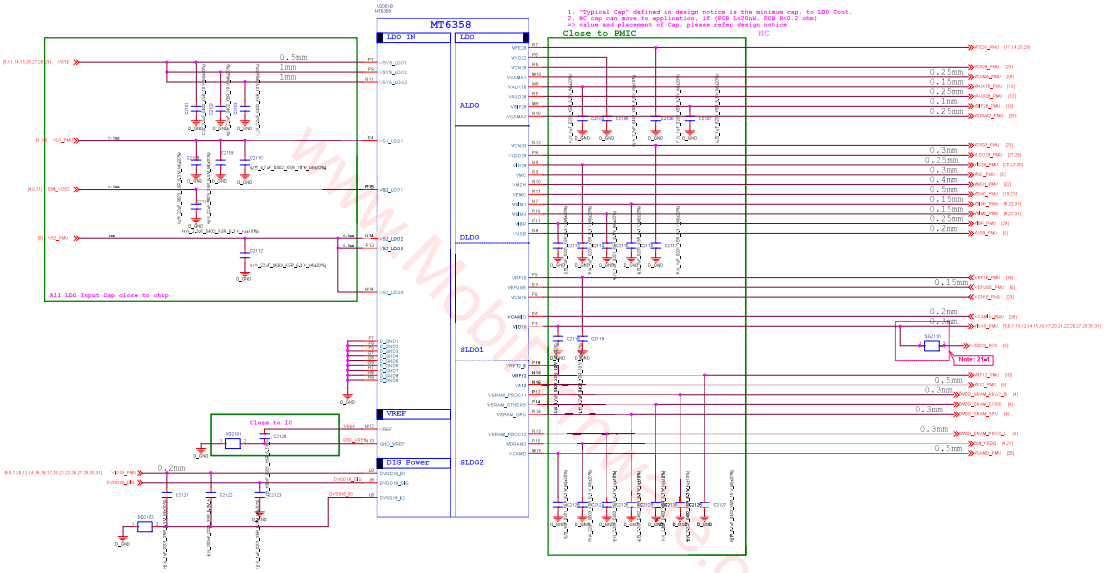

Schematic design notice of "21_POWER_MT6358-LDO" page.

Note 21-1: Please set SG2110 close to C2118, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2118 Please also refer to MT6358 design notice for further detail design information

Note 21-2: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6358 design notice.

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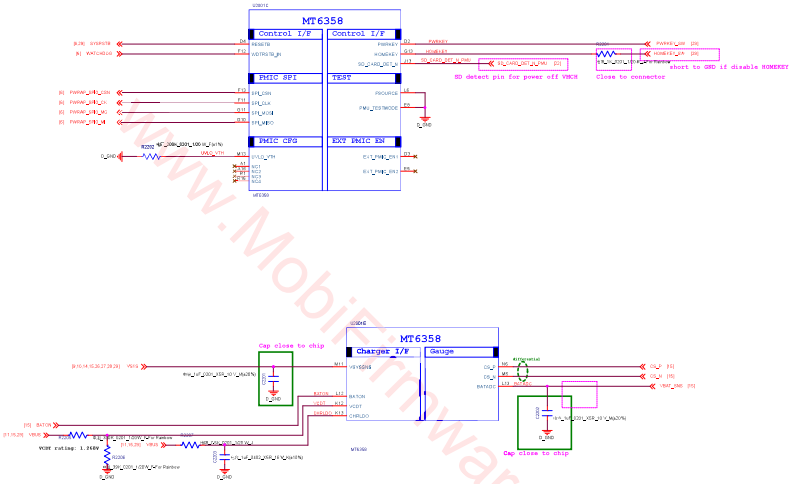

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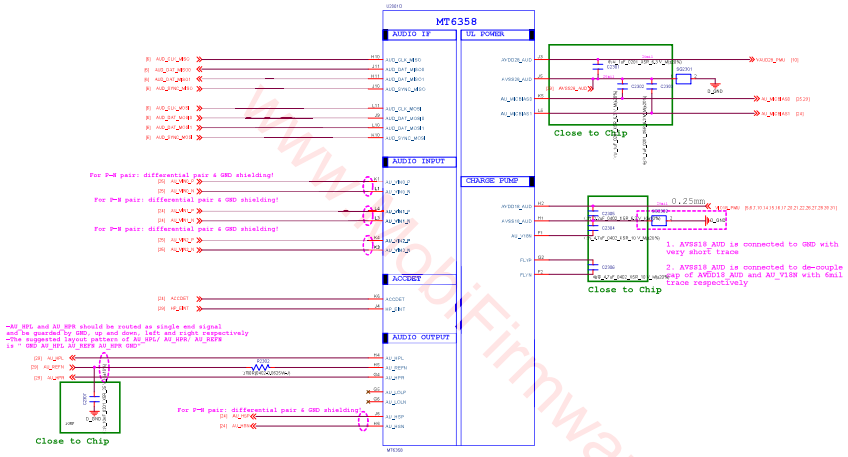

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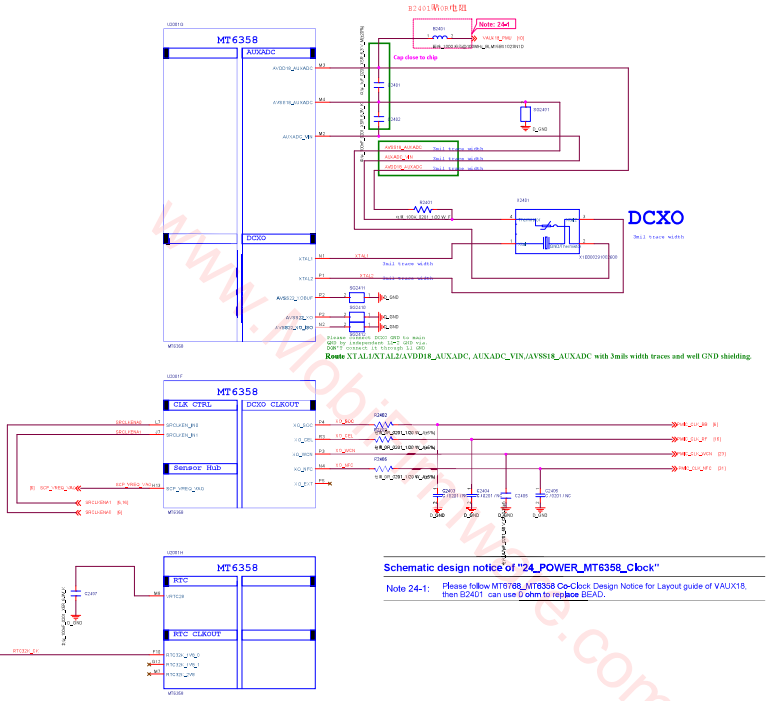

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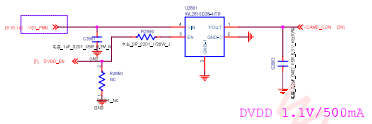
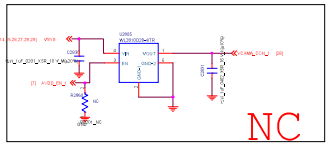
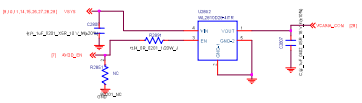
LDO for Rear Camera (VCAMD_EXT1)
1.06V



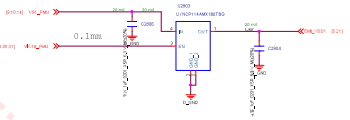
LDO for Dual Camera (VCAMA_EXT)
2.8V



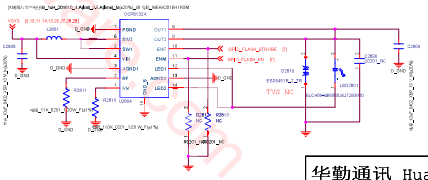
LDO for Dual Camera (VCAMA_EXT)
2.8V



Ext. EMI_VDD1 for LPDDR4X VDD1



Flash LED 5V Boost



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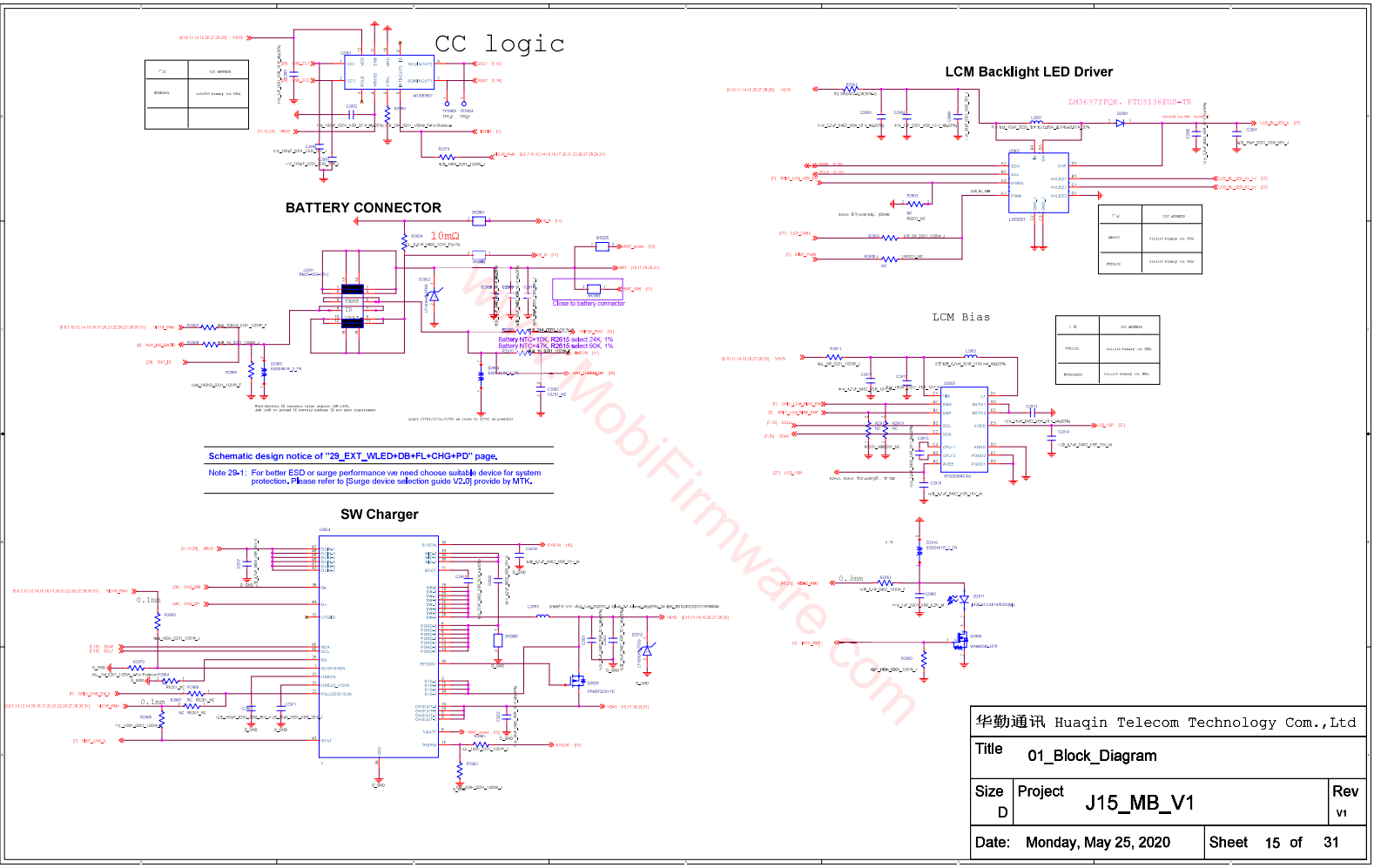

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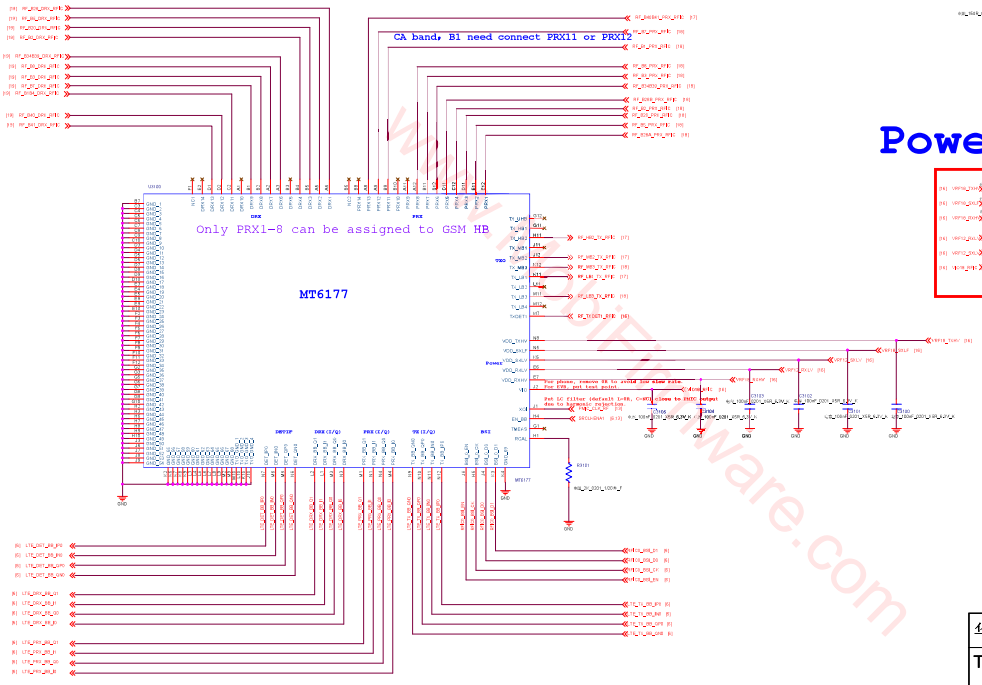
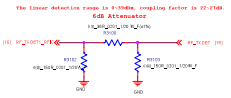
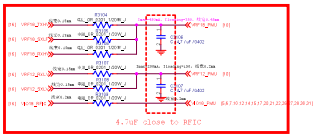
Transceiver



Attenuator for Detector



Power For MT6177



GND

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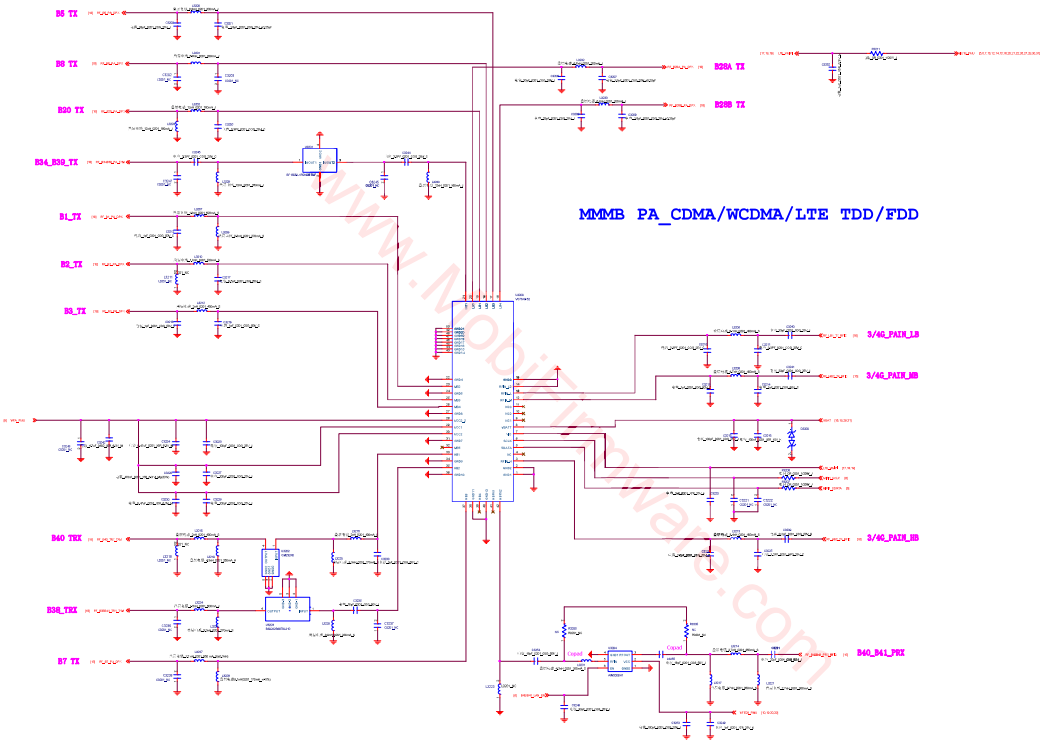

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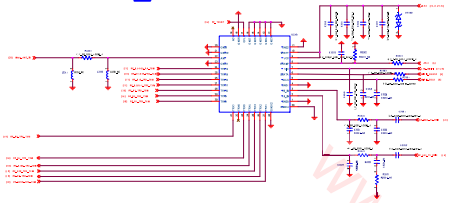
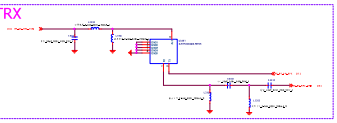
MAIN_ANT

TXM_GSM

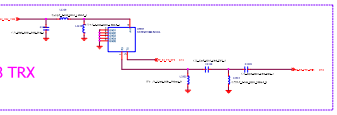


TRX_LB

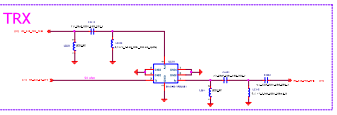
B5 TRX



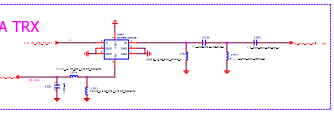
B8 TRX



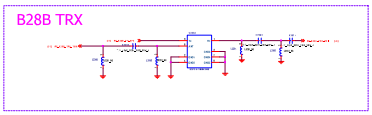
B20 TRX



B28A TRX

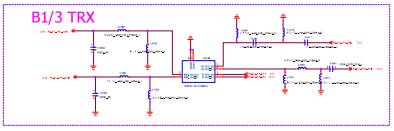


B28B TRX

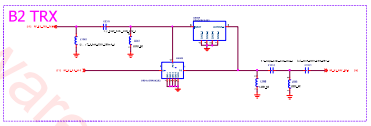


TRX_MB

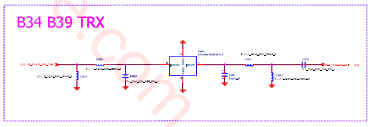
B1/3 TRX



B2 TRX

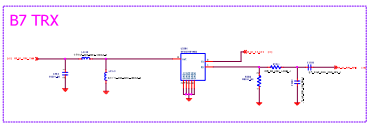


B34 B39 TRX



TRX_HB

B7 TRX



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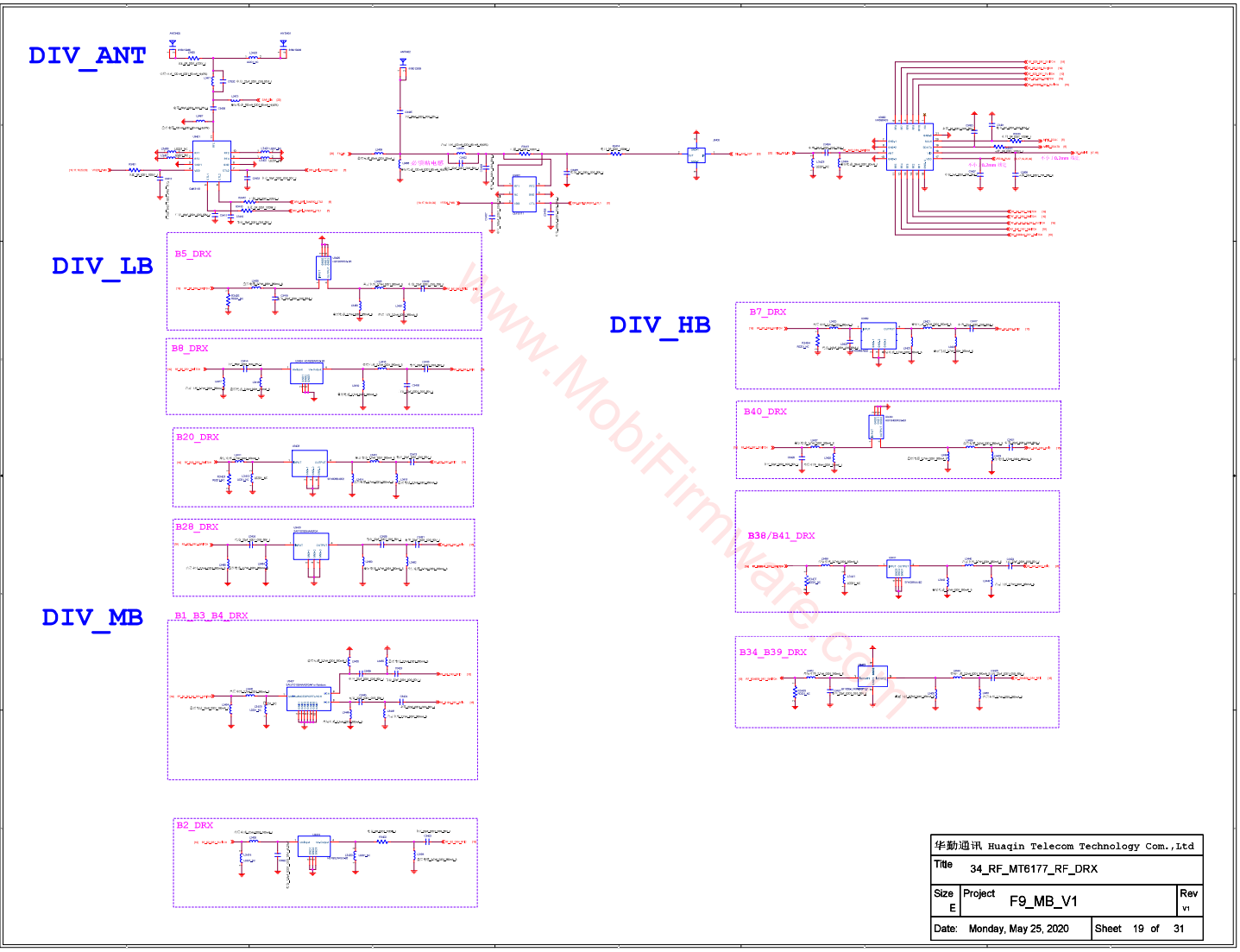

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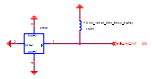
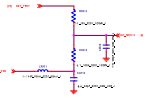
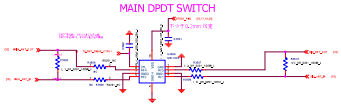


空口检测

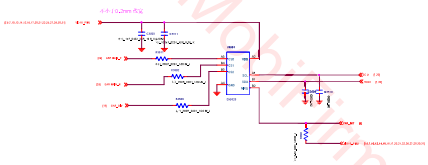


TAS

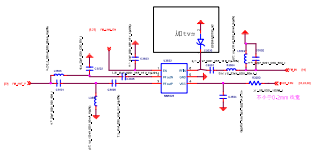
MAIN DPDT SWITCH



SAR Sensor



FM



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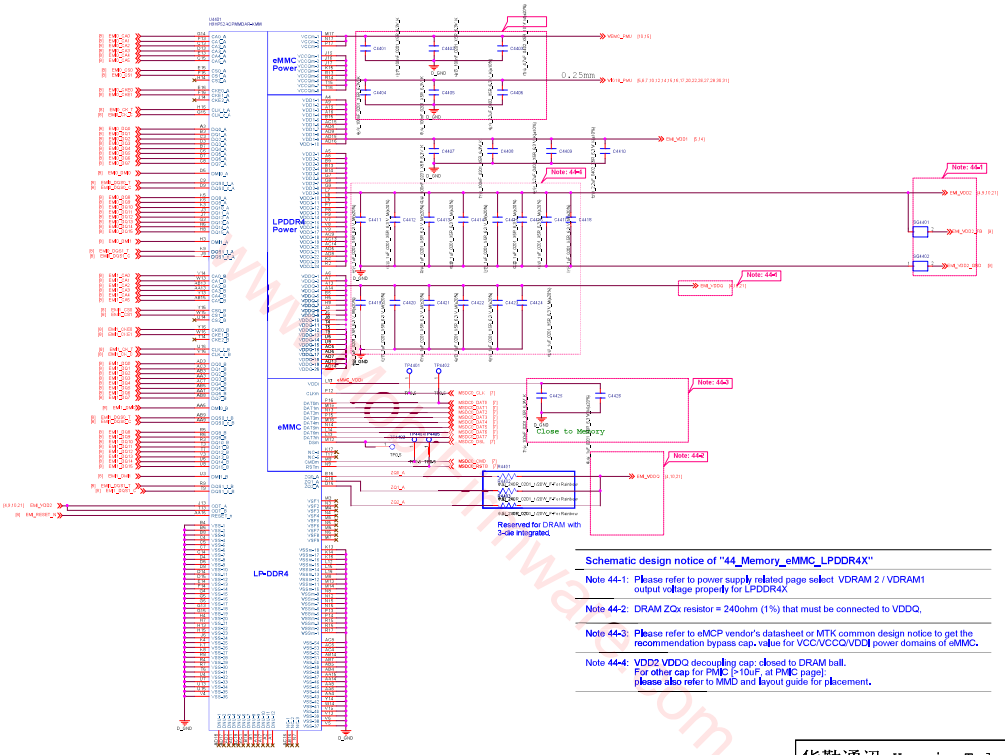

Schematic design notice of "44_Memory_eMMC_LPDDR4X"

Note 44-1: Please refer to power supply related page select VDRAM 2 / VDRAM1 output voltage properly for LPDDR4X

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ.

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page],
please also refer to MMD and layout guide for placement.

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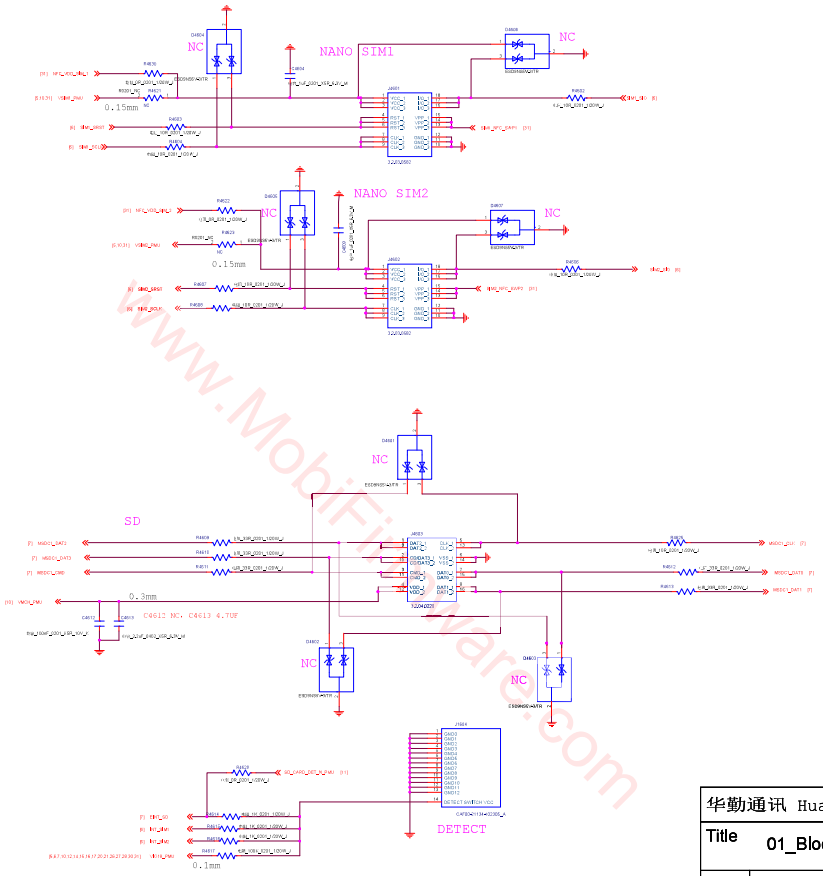

Note 46-1:

Schematic design notice of "46_MEMORY_SD Card" page.

For better ESD performance, please select suitable components for system protection.

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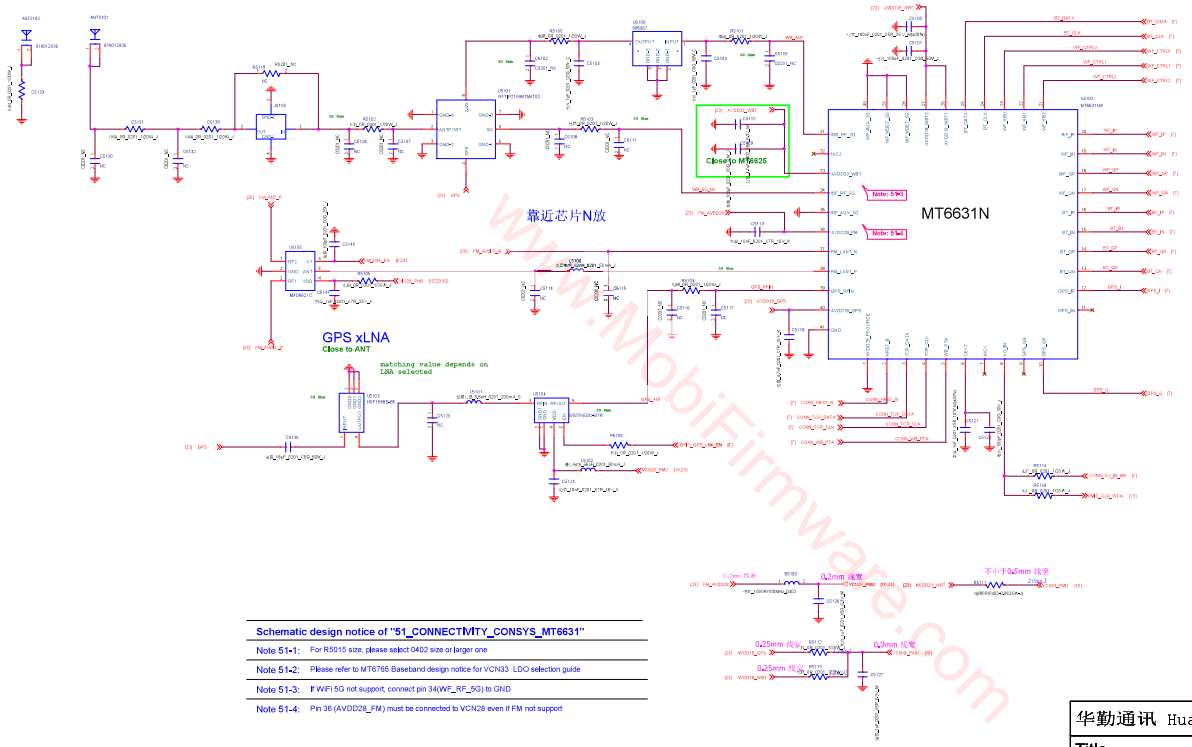

Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"	
Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6765 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support

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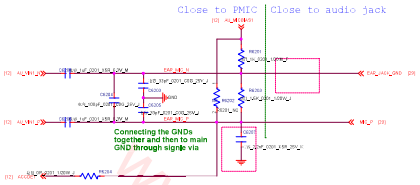
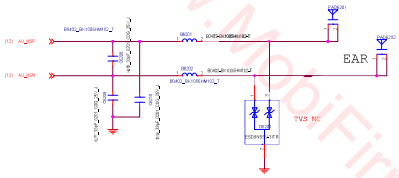
Earphone Microphone





Schematic design notice of "62_PERI_AUDIO_IO" page.

Note 62-1: Part # of BEAD6202, BEAD6203, BEAD6204 and BEAD6205 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

Note 62-2: Reserved Cap for CS/RS test, please double check multi-key function when used

Note 62-3:

	Earphone Jack @ Main board	Earphone Jack @ Sub board
	P-CON	CONN

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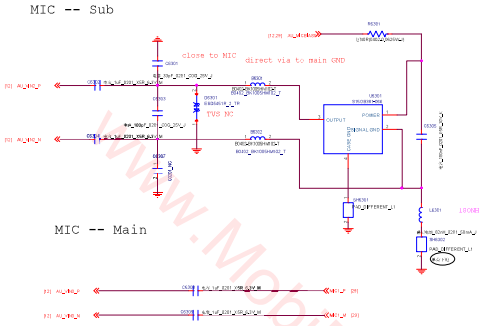

Schematic design notice of "63_PERI_AUDIO_IO" page.

Note 63-1: 1 uF for ACC mode

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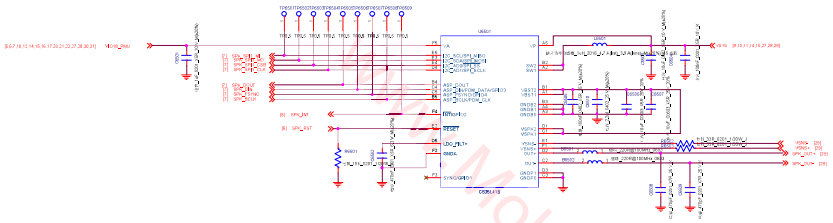
Speaker Amplifier

MT6660 Speaker AMP I2C Address: 0x34 (Write:0x68, Read:0x69) when ADS1 = GND; ADS2 = GND.



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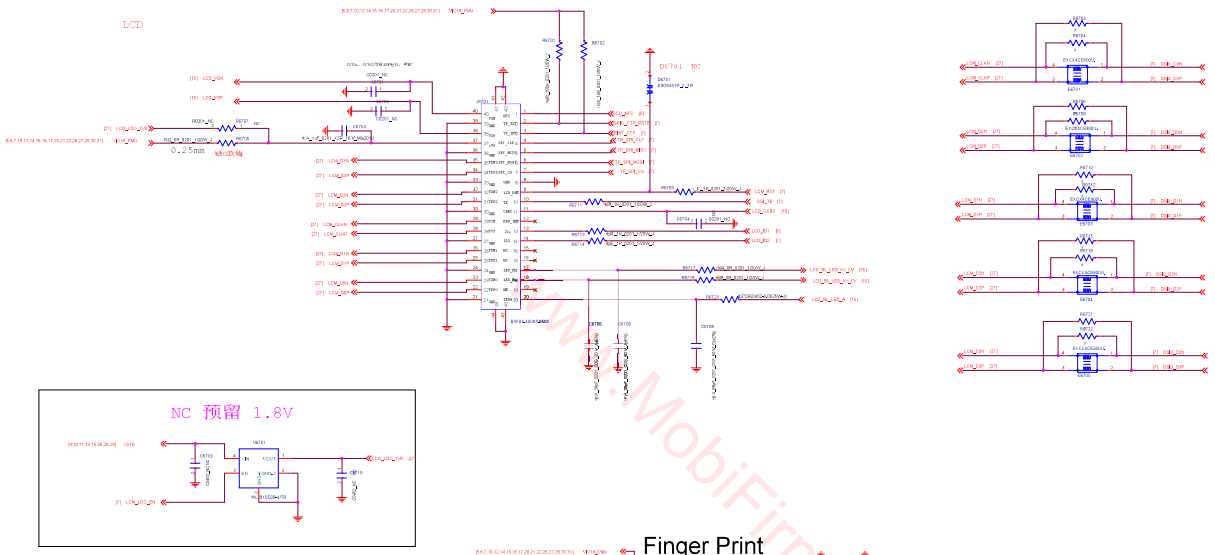

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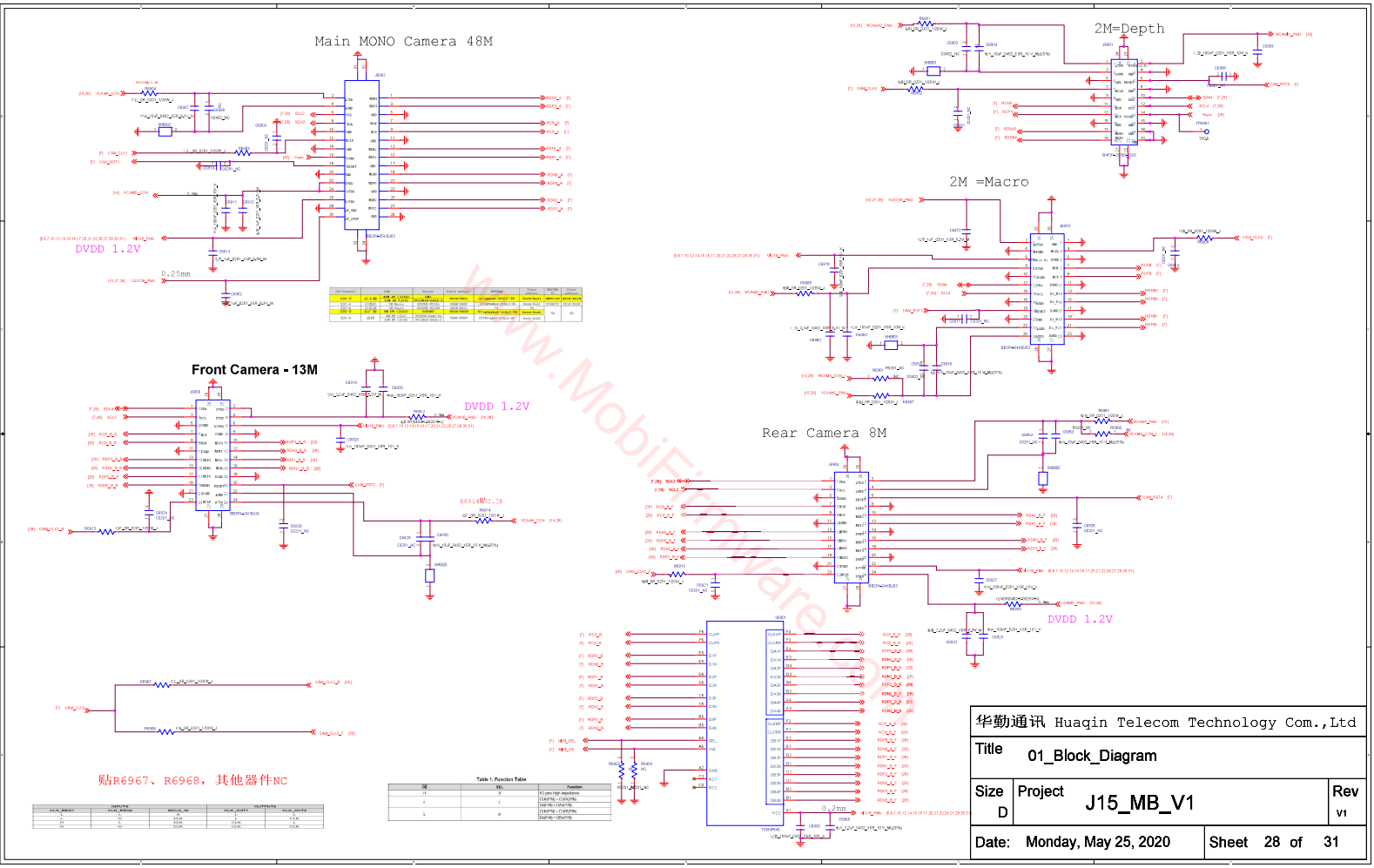

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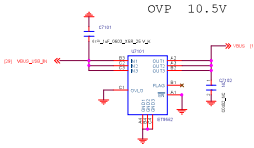
OVP 10.5V ET9552



反向充电开关

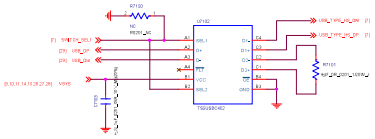
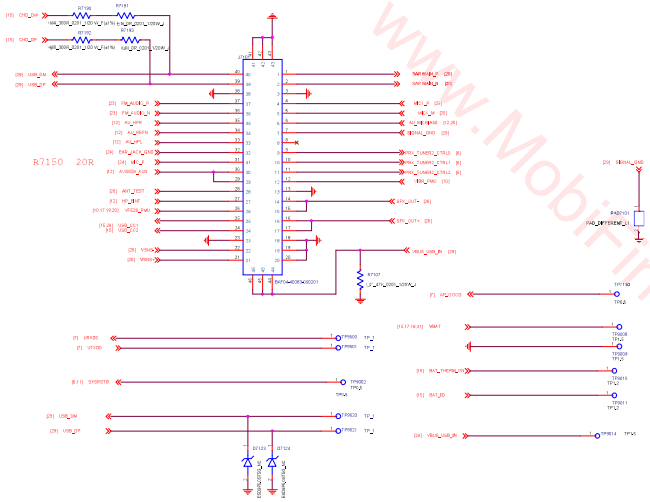


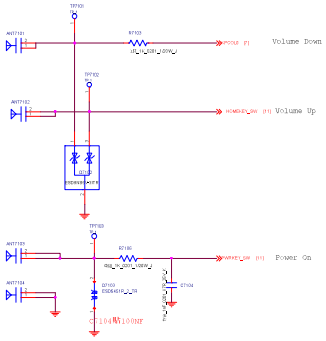
Table 1. Function Table

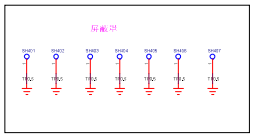
OE	SEL1	SEL2	D- Connection	D+ Connection
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+

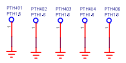
MAIN FPC BTB



KEY BTB







USB

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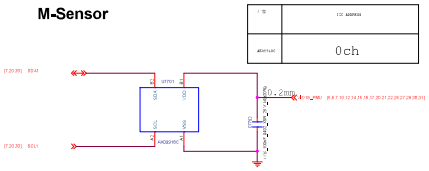
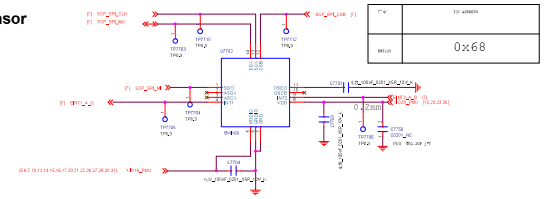
M-Sensor



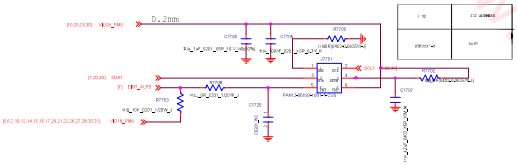
Accerometer + Gyro Sensor

default SPI (if sensor hub support)

Gyro+A sensor



ALS PS STK3337-X



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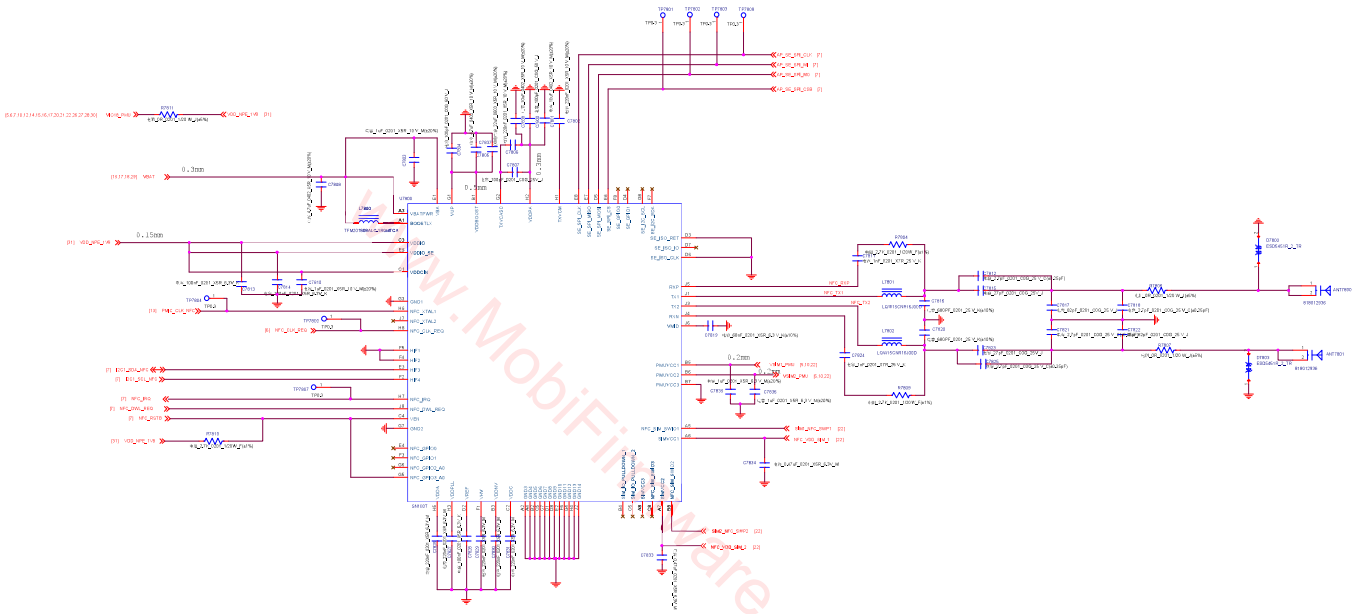

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